What is claimed is:

1. An integrated circuit interconnection comprising:

a transmission line having a low characteristic impedance, said transmission line including a first end and a second end;

a driver coupled to the first end of said transmission line;

a termination at the second end of said transmission line having an impedance corresponding to the characteristic impedance of said transmission line;* and

a plurality of components selected from the group consisting of capacitive elements, inductive elements and a combination of capacitive and inductive elements, said components being connected at spaced intervals to said transmission line between said first and second ends.

2. The integrated circuit interconnection of claim 1 wherein said components change the propagation constant and delay time of said transmission line.

3. The integrated circuit interconnection of claim 1 wherein said components are a plurality of capacitive elements.

4. The integrated circuit interconnection of claim 1 wherein said components are a plurality of inductive elements.

5. The integrated circuit interconnection of claim 1 wherein said components are a combination of capacitive and inductive elements.

6. The integrated circuit interconnection of claim 1 wherein said transmission line has a characteristic impedance of less than 50 Ohms.

7. The integrated circuit interconnection of claim 1 wherein a current sense amplifier is coupled to the second end of the transmission line.

8. The integrated circuit interconnection of claim 1 wherein a plurality of interconnection lines are connected to said transmission line.

9. The integrated circuit interconnection of claim 3 wherein said capacitive elements are selected from the group consisting of metal-metal, metal-polysilicon and polysilicon-polysilicon capacitors.

10. The integrated circuit interconnection of claim 1 wherein said capacitive elements are gate capacitances of field effect transistors used as capacitors.

11. The integrated circuit interconnection of claim 1 wherein said inductive elements are spiral inductors serially

implanted in said transmission line.

12. The integrated circuit interconnection of claim 1 wherein said inductive elements are formed by depositing material with a higher magnetic permeability on said transmission line for increasing self inductance of said transmission line.

13. The integrated circuit interconnection of claim 1 wherein said termination is formed in complementary metal-oxide semiconductor (CMOS) technology on the second end of said transmission line.

14. The integrated circuit interconnection of claim 7 wherein said current sense amplifier which has an input impedance of less than 50 Ohms.

15. The integrated circuit interconnection of claim 1 wherein and a differential receiver is coupled to the second end of the transmission line.

16. The integrated circuit interconnection of claim 1 wherein an amplifier circuit comprising a pair of cross coupled CMOS amplifiers is coupled to the second end of said transmission line.

17. The integrated circuit interconnection of claim 16

wherein each amplifier comprising:

a first transistor of a first conductivity type having a source region, a drain region, and a gate opposing a body region;

a second transistor of a second conductivity type having a source region, a drain region, and a gate opposing a body region;

a signal input node coupled to the source region for the first transistor;

a signal output node coupled to the drain regions for the first transistor and the second transistor; and

a third transistor of a first conductivity type having a source region, a drain region, and a gate opposing a body region, wherein the signal input node is coupled to the gate of the third transistor, wherein the drain region is coupled to a positive voltage supply and the source region is coupled to a lower voltage potential, and wherein the drain region is coupled to the gate of the first transistor;

said second end of said transmission line being coupled to the signal input of a first one of the pair of cross coupled CMOS amplifiers; and

a second transmission line coupled to the signal input of a second one of the pair of cross coupled CMOS amplifiers.

18. The integrated circuit interconnection of claim 17, wherein the first transistor of a first conductivity type includes an n-channel metal-oxide semiconductor (NMOS)

transistor, and wherein the second transistor of a second conductivity type includes a p-channel metal-oxide semiconductor (PMOS) transistor.

19. The integrated circuit interconnection of claim 18, wherein each amplifier in the amplifier circuit includes a fourth transistor of a first conductivity type having a source region, a drain region, and a gate opposing a body region, wherein the drain region is coupled to the source region for the first transistor.

20. The integrated circuit interconnection of claim 19, wherein the signal output node for each amplifier is cross coupled to the gate of the second transistor and the fourth transistor on the other amplifier.

21. The integrated circuit interconnection of claim 16 wherein the signal input node for each amplifier is coupled to a transmission line which has a length of at least 1000 micrometers.

22. The integrated circuit interconnection of claim 16 wherein the signal input node for each amplifier is coupled to a transmission line which has a length of at least 500 micrometers.

23. The integrated circuit interconnection of claim 1

wherein an amplifier circuit is coupled to the second end of said transmission line.

24. The integrated circuit interconnection of claim 13 wherein said amplifier circuit comprises:

a pair of cross coupled transistors;

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to a drain region on each one of the pair of cross coupled transistors; and

a single signal input node coupled to a source region for one of the pair of cross coupled transistors, wherein the amplifier circuit is able to provide a differential voltage signal to the pair of output transmission lines when a single ended input current of less than 1.0 mA is received at the single signal input node.

25. The integrated circuit interconnection of claim 24, wherein each one of the pair of output transmission lines coupled to the drain region on each one of the pair of cross coupled transistors is further coupled to a gate for the other transistor in the pair of cross coupled transistors.

26. The integrated circuit interconnection of claim 25, wherein each transistor in the pair of cross coupled transistors an n-channel metal oxide semiconductor (NMOS) transistor.

27. The integrated circuit interconnection of claim 24, wherein the single signal input node is coupled to a current mirror.

28. The integrated circuit interconnection of claim 1 wherein a pseudo differential amplifier circuit is coupled to the second end of said transmission line.

29. The integrated circuit interconnection of claim 28 wherein said pseudo differential amplifier circuit comprises:

a first pair of metal oxide semiconductor field effect transistors (MOSFETs), wherein the first pair of MOSFETS are cross coupled;

a pair of load resistors, wherein each load resistor is coupled to a drain region for each MOSFET in the first pair of MOSFETs;

a pair of signal output nodes, wherein each one of the pair of signal output nodes is coupled to the drain region for each MOSFET in the first pair of MOSFETs;

a single signal input node coupled to a source region for one of the MOSFETs in the first pair of MOSFETs; and

a second pair of MOSFETs, wherein a drain region for each MOSFET in the second pair of MOSFETs is coupled to a source region of for each MOSFET in the first pair of MOSFETs, and wherein the signal input node is coupled to a gate for each of the second pair of MOSFETs.

30. The integrated circuit interconnection of claim 29, wherein the pseudo differential amplifier is able to provide a different voltage signal to the pair of signal output nodes when current signal of 0.5 mA or less is received at the single signal input node.

31. The integrated circuit interconnection of claim 29 wherein the first pair of MOSFETs includes a first pair of n-channel metal oxide semiconductor (NMOS) transistors.

32. The integrated circuit interconnection of claim 29, wherein the second pair of MOSFETs includes a second pair of n-channel metal oxide semiconductor (NMOS) transistors.

33. The integrated circuit interconnection of claim 29, wherein said transmission line has a characteristic impedance of less than 50 Ohms.

34. The integrated circuit interconnection of claim 29, wherein the drain region for each MOSFET in the first pair of MOSFETs is coupled to a gate of the other MOSFET in the first pair of MOSFETs.

35. The integrated circuit interconnection of claim 1 wherein a single ended amplifier circuit is coupled to the second end of said transmission line.

36. The integrated circuit interconnection of claim 35 wherein said single ended amplifier circuit comprises:

a pair of cross coupled amplifiers, wherein each amplifier comprises:

a load resistor;

a first transistor having a source region, a drain region coupled to the load resistor, and a gate opposing a body region;

a signal output node coupled to the drain region for the first transistor; and

a second transistor having a source region, a drain region, and a gate opposing a body region, wherein the drain region of the second transistor is coupled to the source region of the first transistor; and

a signal input node coupled to the source region for the first transistor in one of the cross coupled amplifiers, wherein the signal input node is further coupled to the gate in each second transistor.

37. The integrated circuit interconnection of claim 36, wherein the single ended amplifier provides an amplified output signal to the output nodes in the pair of cross coupled amplifiers when a 0.5 mA single ended input current is received at the single signal input node.

38. The integrated circuit interconnection of claim 1

wherein a current sense amplifier circuit is coupled through a signal input node to the second end of said transmission line, said current sense amplifier comprising:

a first transistor of a first conductivity type;

a second transistor of a second conductivity type, wherein the first and second transistors are coupled at a drain region; and

said signal input node coupled to a source region of the first transistor; and

a signal output node coupled to the drain region of the first and the second transistor in the second amplifier, and wherein the signal output node is further coupled to a gate of a third transistor.

39. The integrated circuit interconnection of claim 38 wherein a source region of the third transistor is coupled to a source region of the second transistor, and wherein a drain region of the third transistor is coupled to the signal input.

40. The current sense amplifier of claim 38, wherein the first transistor of a first conductivity type includes an n-channel metal oxide semiconductor (NMOS) transistor, and wherein the second transistor of a second conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor.

41. The current sense amplifier of claim 38, wherein the

drain region for the first and the second transistor in the first amplifier are coupled to gates of the second transistor in the first and the second amplifier.

42. The current sense amplifier of claim 38, wherein the third transistor is an n-channel metal oxide semiconductor (NMOS) transistor.

43. The current sense amplifier of claim 38, wherein the signal input node of the first amplifier receives an input current, and wherein the signal input node of the second amplifier receives a reference current.

44. An integrated circuit interconnection for minimizing clock skews comprising:

a transmission line having a low characteristic impedance, said transmission line including a first end and a second end;

a driver coupled to the first end of said transmission line;

a termination at the second end of said transmission line having an impedance corresponding to the characteristic impedance of said transmission line for reducing ringing and reflections, said termination including a current sense amplifier coupled to the second end of the transmission line; and

a plurality of components selected from the group

consisting of capacitive elements, inductive elements and a combination of capacitive and inductive elements, said components being connected at spaced intervals to said transmission line between said first and second ends for changing the propagation constant and delay time of said transmission line.

45. The integrated circuit interconnection of claim 44 wherein said components are a plurality of capacitive elements.

46. The integrated circuit interconnection of claim 44 wherein said components are a plurality of inductive elements.

47. The integrated circuit interconnection of claim 44 wherein said components are a combination of capacitive and inductive elements.

48. The integrated circuit interconnection of claim 44 wherein said transmission line has a characteristic impedance of less than 50 Ohms.

49. The integrated circuit interconnection of claim 44 wherein a current sense amplifier is coupled to the second end of the transmission line.

50. The integrated circuit interconnection of claim 44

wherein a plurality of interconnection lines are connected to said transmission line.

51. The integrated circuit interconnection of claim 45 wherein said capacitive elements are selected from the group consisting of metal-metal, metal-polysilicon and polysilicon-polysilicon capacitors.

52. The integrated circuit interconnection of claim 45 wherein said capacitive elements are gate capacitances of field effect transistors used as capacitors.

53. The integrated circuit interconnection of claim 46 wherein said inductive elements are spiral inductors serially implanted in said transmission line.

54. The integrated circuit interconnection of claim 46 wherein said inductive elements are formed by depositing material with a higher magnetic permeability on said transmission line for increasing self inductance of said transmission line.

55. The integrated circuit interconnection of claim 49 wherein said current sense amplifier which has an input impedance of less than 50 Ohms.

56. A method for minimizing clock skews on integrated

circuit interconnections comprising the steps of:

providing a transmission line having a low characteristic impedance, said transmission line including a first end and a second end;

coupling a driver to the first end of said transmission line;

coupling the second end of the transmission line to a current sense amplifier having an input impedance corresponding to the characteristic impedance of said transmission line for reducing ringing and reflections; and

connecting a plurality components at spaced intervals to said transmission line between said first and second ends for changing the propagation constant and delay time of said transmission line, said components being selected from the group consisting of capacitive elements, inductive elements and a combination of capacitive and inductive elements.

57. The method of claim 56 wherein said components are a plurality of capacitive elements.

58. The method of claim 56 wherein said components are a plurality of inductive elements.

59. The method of claim 56 wherein said components are a combination of capacitive and inductive elements.

60. The method of claim 56 wherein said transmission

line has a characteristic impedance of less than 50 Ohms.

61. The method of claim 56 further comprising connecting a plurality of interconnection lines to said transmission line.

62. The method of claim 57 wherein said capacitive elements are selected from the group consisting of metal-metal, metal-polysilicon and polysilicon-polysilicon capacitors.

63. The method of claim 57 wherein said capacitive elements are gate capacitances of field effect transistors used as capacitors.

64. The method of claim 58 wherein said inductive elements are spiral inductors serially implanted in said transmission line.

65. The method of claim 58 wherein said inductive elements are formed by depositing material with a higher magnetic permeability on said transmission line for increasing self inductance of said transmission line.

66. The method of claim 56 wherein said current sense amplifier which has an input impedance of less than 50 Ohms.